DETAILED ACTION

This Examiner's Amendment and Examiner's Reasons for Allowance action is in response to the filing of 12/01/2009.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Roland McAndrews on 03/25/2010.

- The application has been amended as follows:

Claim 1 (Currently Amended) A computer that is configured for connection to a network including the Internet, comprising:

a microchip including a microprocessor, said microprocessor including a master control unit and at least two processing units, the master control unit [[being]] configured to control the processing units;

at least one Faraday Cage [[substantially]] surrounding said microchip;

said microchip further including at least on inner firewall, located between the master control unit and the at least two processing units, configured with hardware to make the master

control unit and one of the processing units inaccessible from the network including the Internet when the computer is connected to the network including the Internet; and

said at least one inner firewall is further configured in a manner that permits access by another computer in the network including the Internet to at least one of the processing units of the microprocessor for an operation with said another computer in the network including the Internet when the computer is connected to the network including the Internet.

Claim 10 (Currently Amended) A computer that is configured for connection to a network including the Internet, comprising:

a microchip including a microprocessor, said microprocessor including a master control unit that is configured using hardware and firmware and including at least two processing units, the master control unit [[being]] further configured to control the processing units;

a Faraday Cage [[substantially]] surrounding said microchip;

said microchip including at least two inner firewalls;

a first of said at least two inner firewalls, located between the master control unit and a first one of the at least two processing units, is configured with hardware to make the master control unit and the first one of the processing units inaccessible from the network including the Internet when the computer is connected to the network including the Internet; and

a second of said at least two inner firewalls, located between the master control unit and a second one of the at least two processing units, is configured with hardware to make the second one of the processing units of the microprocessor inaccessible from the network including the Internet when the computer is connected to the network including the Internet.

Claim 50 (Currently Amended) A computer that is configured for connection to a network including the Internet, comprising:

a microchip including a microprocessor, at least two inner firewalls and at least two memory components,

said microprocessor including a master control unit that is configured using hardware and firmware and including at least two processing units, the master control unit [[being]] configured to control the processing units;

a Faraday Cage [[substantially]] surrounding said microchip;

a first of at least two inner firewalls, located between the master control unit and a first of said at least two processing units, is configured with hardware to make the master control unit, said first of said at least two processing units and a first of said at least two memory components inaccessible from the network including the Internet when the computer is connected to the network including the Internet; and

a second of said at least two inner firewalls, located between the master control unit and a second of said at least two processing units, is configured with hardware to make the second of said at least two processing units and a second of said at least two memory components inaccessible from the network including the Internet when the computer is connected to the network including the Internet.

Claim 73 (Currently Amended) A computer that is configured for connection to a network including the Internet, comprising:

a microchip including a microprocessor, at least two inner firewalls and at least two memory components,

said microprocessor including a master control unit that is configured using hardware and firmware and including at least two processing units, the master control unit [[being]] configured to control the processing units;

a Faraday Cage [[substantially]] surrounding said microchip;

a first of said at least two inner firewalls, located between the master control unit and a first of said at least two memory components, is configured with hardware to make the master control unit, one of the processing units, and the first of said at least two memory components inaccessible from the network including the Internet when the computer is connected to the network including the Internet; and

a second of said at least two inner firewalls, located between the master control unit and a second of said at least two memory components, is configured with hardware to make the second of said at least two memory components inaccessible from the network including the Internet when the computer is connected to the network including the Internet.

Claim 80 (Currently Amended) A computer that is configured for connection to a network including the Internet, comprising:

a microchip including a microprocessor, including a master control unit that is configured using hardware and firmware, at least two processing units and at least one inner firewall, the master control unit [[being]] configured to control the processing units;

at least one photovoltaic cell located on said microchip; and

said at least one inner firewall, located between the master control unit and the at least two processing units, is configured with hardware to make the master control unit and one of the processing units inaccessible from the network including the Internet when the computer is connected to the network including the Internet.

Claim 82 (Currently Amended) A computer that is configured for connection to a network including the Internet, comprising:

a microchip including a microprocessor, including a master control unit that is configured using hardware and firmware, at least two processing units and at least one inner firewall, the master control unit [[being]] configured to control the processing units;

at least one photovoltaic cell located on said microchip; and

a Faraday Cage [[substantially]] surrounding said microchip;

wherein said at least one firewall, located between the master control unit and the at least two processing units, is configured with hardware to make the master control unit and one of the processing units inaccessible from the network including the Internet when the computer is connected to the network including the Internet.

Allowance

2. Claims 8, 9, 23, 28, 31, 32, 40, 62, 74, 75, & 78 have been cancelled.

3. Claims 1-7, 10-22, 24-27, 29, 30, 33-39, 41-61, 63-73, 76, 77, & 79-105 have been amended with written arguments which overcome the examiner's prior rejections and objections, see paper of 07/01/2009. Examiner withdraws all outstanding rejections and objections to Claims 1-7, 10-22, 24-27, 29, 30, 33-39, 41-61, 63-73, 76, 77, & 79-105.

4. Claims 1-7, 10-22, 24-27, 29, 30, 33-39, 41-61, 63-73, 76, 77, & 79-105 are allowed.

Examiner's Statement of Reasons for Allowance

5. Prior art was found which disclosed photovoltaic cell attached to microchip [e.g. Hornstein et al. (US-5905429-A)] and apparatus and method for inhibiting electromagnetic interference [e.g. Alina et al. (US-6366472)] and duplicate control and processing unit for telecommunications equipment [e.g. De Leva et al. (US-5784551)] and network firewalls [e.g. McKelvey (US-5896499-A)] and EMI shield [e.g. Bright et al. (US-5357404-A)] and system for sharing network state to enhance network throughput [e.g. Purtell et al. (US-6950947-B1)] and processor card assembly including a heat sink attachment plate and an EMI/ESD shielding cage [e.g. Nelson et al. (US-5838542-A)] and cellular communications system with centralized base stations and distributed antenna units [e.g. Russell et al. (US-5627879-A)] and methods and apparatus for CDMA wireless call setup time/service negotiation optimization [e.g. Boulos et al. (US-6208634-B1)] and data storage controller providing multiple hosts with access to multiple storage subsystems [e.g. Bergsten (US-6073209-A)] and method and system for controlling power consumption in a computer system [e.g. Reneris (US-5784628-A)] and method and

apparatus for creating a security environment for a user task in a client/server system [e.g. Ault et al. (US-5764889-A)] and computer security system [e.g. Lapointe et al. (US-5606615-A)] and system for, and method of, displaying prices on tags in supermarkets [e.g. Palmer et al. (US-5861817-A)].

6. The following is an examiner's statement of reasons for allowance:

- The prior art of record does not teach or render obvious the limitations as recited in independent Claims 1, 10, 50, 73, 80, & 82, specific to "a microchip including a microprocessor, said microprocessor including a master control unit and at least two processing units, the master control unit configured to control the processing units" and "said microchip further including at least on inner firewall, located between the master control unit and the at least two processing units, configured with hardware to make the master control unit and one of the processing units inaccessible from the network including the Internet when the computer is connected to the network including the Internet" and "said at least one inner firewall is further configured in a manner that permits access by another computer in the network including the Internet to at least one of the processing units of the microprocessor for an operation with said another computer in the network including the Internet when the computer is connected to the network including the Internet" and "at least one photovoltaic cell located on said microchip" and "a microchip including a microprocessor, at least two inner firewalls and at least two memory components."
- Dependent claims are allowed as they depend from an allowable independent claim.

- Therefore, the Examiner considers both the above limitations in combination with the remaining limitations as found in each respective independent claim, as applied to a microchip secured with at least one internal firewall between the master control unit and processing unit(s) of the microprocessor, as the non-obvious novelties of the invention.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Friday from 8:30 AM to 5:00 PM. The examiner can also be contacted via E-mail to schedule a telephone discussion at OSCAR.LOUIE@USPTO.GOV.

If attempts to reach the examiner by telephone or E-mail are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2400 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is only available through Private PAIR. If you have questions on access to the

Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 571-272-4100 (local). For more information on the PAIR system or the EBC please visit http://www.uspto.gov/patents/ebc/index.jsp. If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000 (local).

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03/26/2010

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